IN THE CLAIMS

1 (Original). An apparatus comprising:

a plurality of signal-processing stages, each signal processing stage having an output coupled to an interstage summing node;

a quantizer coupled between an interstage summing node and a digital output node; and

a multilevel quantized feedback stage having an input coupled to the output node and an output coupled to interstage summing nodes, the feedback stage comprising an analog-trimmed nonvolatile reference circuit.

2 (Original). An apparatus as defined in Claim 1, wherein the feedback stage comprises a multibit digital-to-analog converter (DAC).

3 (Original). An apparatus as defined in Claim 2, wherein the feedback stage comprises a plurality of analog nonvolatile reference current sources.

4 (Original). An apparatus as defined in Claim 3, wherein each of the reference current sources comprises a floating-gate metal-oxide-semiconductor (MOS) transistor.

5 (Original). An apparatus as defined in Claim 4, wherein the reference current sources are constructed to be trimmed by adjustment of a respective voltage applied to a control electrode of each of the MOS transistors.

6 (Original). An apparatus as defined in Claim 1, wherein the feedback stage further comprises a digital-to-analog converter (DAC) coupled to the analog-trimmed nonvolatile reference circuit to effect linearity trimming of the feedback stage.

7 (Previously Amended). An apparatus as defined in Claim 6, wherein the DAC comprises a plurality of analog-trimmed, nonvolatile reference current sources.

8 (Original). An apparatus as defined in Claim 7, wherein each of the reference current sources comprises a floating-gate metal-oxide-semiconductor transistor.

9 (Original). An apparatus as defined in Claim 8, wherein the reference current sources are constructed to be trimmed by application of a respective voltage to one or more of the MOS transistors so as to vary a respective threshold voltage.

10 (Currently Amended). A system comprising:

a plurality of signal-processing stages, each signal-processing stage having an output coupled to an interstage summing node;

a quantizer coupled between an interstage summing node and a digital output node;

a multilevel quantized feedback stage having an input coupled to the output node and an output coupled to interstage summing nodes, the feedback stage comprising an analog-trimmed nonvolatile reference circuit; and

an antenna coupled to the [[data converter]] signal-processing stages.

11 (Original). A system as defined in Claim 10, wherein the feedback stage comprises a multibit, current-mode digital-to-analog converter (DAC).

12 (Original). A system as defined in Claim 11, wherein the DAC comprises a plurality of analog nonvolatile reference current sources.

13 (Original). A system as defined in Claim 12, wherein each of the reference current sources comprises a floating-gate metal-oxide-semiconductor (MOS) transistor.

14 (Original). A system as defined in Claim 13, wherein the reference current sources are constructed to be trimmed by adjustment of a respective voltage applied to a gate electrode of each of the MOS transistors.

15 (Original). A system as defined in Claim 11, wherein the feedback stage comprises a plurality of analog, nonvolatile reference current sources.

16 (Original). A system as defined in Claim 15, wherein each of the reference current sources comprises a floating-gate metal-oxide-semiconductor (MOS) transistor.

17 (Original). A system as defined in Claim 16, wherein the reference current sources are constructed to be trimmed by adjustment of a respective voltage applied to a gate electrode of each of the MOS transistors.

18 (Original). A system as defined in Claim 16, wherein reference current sources are trimmed by application of a voltage to one or more of the MOS transistors so as to vary a respective threshold voltage.

19 (Original). In a sigma-delta data converter, a method of trimming a multilevel quantized feedback stage, the method comprising:

trimming a most significant bit (MSB) reference current source by combining currents provided by other reference current sources to form a lower-order combined current;

comparing a current provided by the MSB reference current source to the lower-order combined current; and

adjusting the MSB reference current source to provide a reference current that substantially matches the lower-order combined current.

20 (Original). A method as defined in Claim 19, wherein the MSB reference current source comprises an analog nonvolatile semiconductor device and the MSB reference current source is adjusted by applying a voltage to a control node of the device in a manner that causes the MSB reference current source to provide a current that substantially matches the lower-order combined current.

21 (Original). A method as defined in Claim 20, further comprising trimming the MSB reference current source upon occasions when the sigma-delta data converter is activated.

22 (Original). A method as defined in Claim 19, further comprising:

comparing a least significant bit (LSB) reference current source to a current provided by a nominal source; and

adjusting the LSB current source to provide a current that substantially matches the current provided by the nominal source.

23 (Original). A method as defined in Claim 22, further comprising:

combining currents provided by the nominal current source and first LSB reference current source to form a first combined current;

comparing a current provided by a second LSB reference current source to the first combined current.

24 (Original). A method as defined in Claim 23, wherein the LSB reference current source comprises an analog nonvolatile semiconductor device and the LSB reference current source is adjusted by applying a voltage to a control node of the device in a manner that causes the LSB reference current source to provide a current that substantially matches the lower-order combined current.

25 (Original). An article comprising a machine-readable stage medium containing instructions that, if executed, enable a system to trim a most significant bit (MSB) reference current source by combining currents provided by other reference current sources to form a lower-order combined current, comparing a current provided by the MSB reference current source to the lower-order combined current, and adjusting the MSB reference current source to provide a reference current that substantially matches the lower-order combined current.

26 (Original). An article as defined in Claim 25, wherein the MSB reference current source comprises an analog nonvolatile semiconductor device and wherein the article further comprises instructions that, if executed, enable the system to adjust the MSB reference current source by application of a voltage to a control node of the device in a manner that causes the MSB reference current source to provide a current that substantially matches the lower-order combined current.

27 (Original). An article as defined in Claim 26, further comprising instructions that, if executed, enable the system to trim the MSB reference current source upon occasions when the multilevel quantified feedback stage is activated.

28 (Original). An article as defined in Claim 25, further comprising instructions that, if executed, enable the system to:

compare a least significant bit (LSB) reference current source to a current provided by a nominal source; and

adjust the LSB current source to provide a current that substantially matches the current provided by the nominal source.

29 (Original). An article as defined in Claim 28, further comprising instructions that, if executed, enable the system to:

combine currents provided by the nominal current source and LSB reference current source to form a first combined current; and

compare a current provided by a second LSB reference current source to the first combined current.

30 (Original). An article as defined in Claim 29, wherein the LSB reference current source comprises an analog nonvolatile semiconductor device and the LSB reference current source is adjusted by application of a voltage to a control node of the device in a manner that causes the LSB reference current source to provide a current that substantially matches the lower-order combined current.